a first gate electrode disposed on the first, second, and third channel regions and along the first source electrode and the first drain electrode, and bent at first and second bending positions; and

a second semiconductor element on the first, second, and third active regions adjacent to the first semiconductor element, including

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fourth, fifth, and sixth channel regions serially connected, adjacent channel regions having width directions essentially perpendicular to each other, the fourth, fifth, and sixth channel regions being adjacent to the first, second, and third channel regions, respectively, with one of the first source electrode and the first drain electrode therebetween,

a second source electrode and a second drain electrode in ohmic contact with the first, second, and third active regions, one of the second source electrode and the second drain electrode and opposing the first drain electrode or the first source electrode across the fourth, fifth, and sixth channel regions, and

a second gate electrode on the fourth, fifth, and sixth channel regions and along one of the second source electrode and the second drain electrode, and bent at third and fourth bending positions, wherein the first insulating region is under the first and third bending positions of the first and second gate electrodes, and the second insulating region is under the second and fourth bending positions of the first and second gate electrodes.